CLAIM AMENDMENTS

1. (previously presented) A semiconductor device comprising:

a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads, each of said bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction substantially perpendicular to said straight line, wherein said plurality of bonding pads comprises a first group of bonding pads with said first regions in a first direction and said second regions in a second direction, and a second group of bonding pads provided with said second regions in said first direction and said first regions in said second direction,

a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip,

a plurality of conductor wires that electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors, and

an encapsulating member that encapsulates said semiconductor chip and said plurality of conductor wires.

2. (previously presented) The semiconductor device according to claim 1 wherein said first and second groups of bonding pads are alternately arranged.

3. (previously presented) The semiconductor device according to claim 1 wherein said plurality of bonding pads are rectangular in shape with their short sides lying in a direction along the edges of said semiconductor chip.

4. (previously presented) The semiconductor device according to claim1 wherein said plurality of bonding pads are formed with the width of said first

region being wider than the width of said second region in the direction along the edges of said semiconductor chip.

5. (previously presented) The semiconductor device according to claim 1 wherein said plurality of bonding pads have notches between said first region and said second region.

6. (previously presented) The semiconductor device according to claim 1 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

7. (previously presented) A method of manufacturing semiconductor devices comprising:

disposing roughly upon a straight line on a semiconductor chip a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line, wherein said plurality of bonding pads comprises a first group of bonding pads with said first regions in a first direction and said second regions in a second direction, and a second group of bonding pads provided with said second regions in said first direction and said first regions in said second direction,

providing a member with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals, and a securing area for securing said semiconductor chip, and

disposing a plurality of conductor wires to electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors.

8. (previously presented) The method of manufacturing semiconductor devices according to claim 7 wherein said first and second groups of bonding pads are alternately arranged.

9. (original) The method of manufacturing semiconductor devices according to claim 8 wherein said connection step comprises: a first step wherein said first region of said plurality of first bonding pads are connected by conductor wire to said third regions of said plurality of conductors, and a second step wherein said first region of said plurality of second bonding pads are connected by conductor wire to said third regions of said plurality of conductors.

10. (previously presented) The method of manufacturing semiconductor devices according to claim 7 further comprising a step wherein, prior to securing said semiconductor chip to said securing area, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

11. (currently amended) The semiconductor device according to claim 2 wherein said plurality of bonding pads are rectangular in shape with their ~~with their~~ short sides lying in a direction along the edges of said semiconductor chip.

12. (previously presented) The semiconductor device according to claim 2 wherein said plurality of bonding pads are formed with the width of said first region being wider than the width of said second region in the direction along the edges of said semiconductor chip.

13. (previously presented) The semiconductor device according to claim 2 wherein said plurality of bonding pads have notches between said first region and said second region.

14. (previously presented) The semiconductor device according to claim 2 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

15. (previously presented) The semiconductor device according to claim 3 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

16. (previously presented) The semiconductor device according to claim 4 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

17. (previously presented) The semiconductor device according to claim 5 wherein said member is an insulating substrate upon one surface of which said semiconductor chip is secured by adhesive, said external connection terminals are roughly spherical terminals formed on the other surface of said substrate, said encapsulating member is resin that encapsulates said semiconductor chip and said plurality of conductor wires on one surface of said substrate, and the lands as said third regions are electrically connected to said roughly spherical terminals via through holes.

18. (previously presented) The method of manufacturing semiconductor devices according to claim 8 further comprising a step wherein, prior to securing said semiconductor chip to said securing area, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

19. (previously presented) The method of manufacturing semiconductor devices according to claim 9 further comprising a step wherein, prior to said securing said semiconductor chip to said securing area, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

20. (currently amended) A semiconductor device; comprising:

a plurality of bond pads arranged on a semiconductor chip, each of said bond pads in said plurality comprising a bond region and a probe region, said plurality of bond pads comprising two groups of bond pads, a first group of bond pads arranged with bond regions in a first direction and probe regions in a second direction, and a second group of bond pads arranged with probe regions in said first direction and bond regions in said second direction, wherein said first and second groups are arranged in an alternating manner with each member of said first group adjacent a member of said second group, and with the probe region of each said member of said first group adjacent the

bond region of said adjacent member of said second group.